

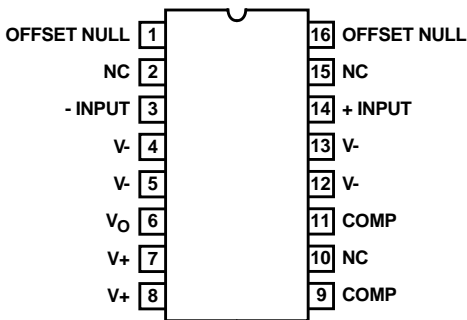
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NO RECOMMENDED REPLACEMENT  
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or email: centapp@harris.com**

**220MHz, Video Line Driver, High Speed Operational Amplifier**

The CA3450 is a large signal video line driver and high speed operational amplifier capable of driving 50Ω transmission lines and flash A/Ds. The uncompensated unity gain crossing occurs at 230MHz without load. It can operate at dual or single supplies of ±7.25V or 14.5V, respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75mA SINK or SOURCE. The CA3450 is capable of driving Flash A/Ds in video or high speed instrumentation (accurate) applications with bandwidth up to 10MHz. Offset voltage nulling terminals are also available.

**Pinout**

**CA3450  
(PDIP)  
TOP VIEW**



**Features**

- High Open Loop Gain at Video Frequencies  
-  $A_{OL} > 40dB$  at  $f = 5MHz$
- Power Bandwidth of 10MHz . . . . .  $A_{CL} = 5; V_O = \pm 3.5V$
- Slew Rate at Full Load . . . . .  $330V/\mu s (A_V \ge 10)$
- $f_T = 220MHz; C_C = 0pF$  With a Load of  $50\Omega || 20pF || 1M\Omega$  (Scope Input)
- $V_{OUT} = \pm 4.1V$  Into  $75\Omega$
- Offset Null Terminals

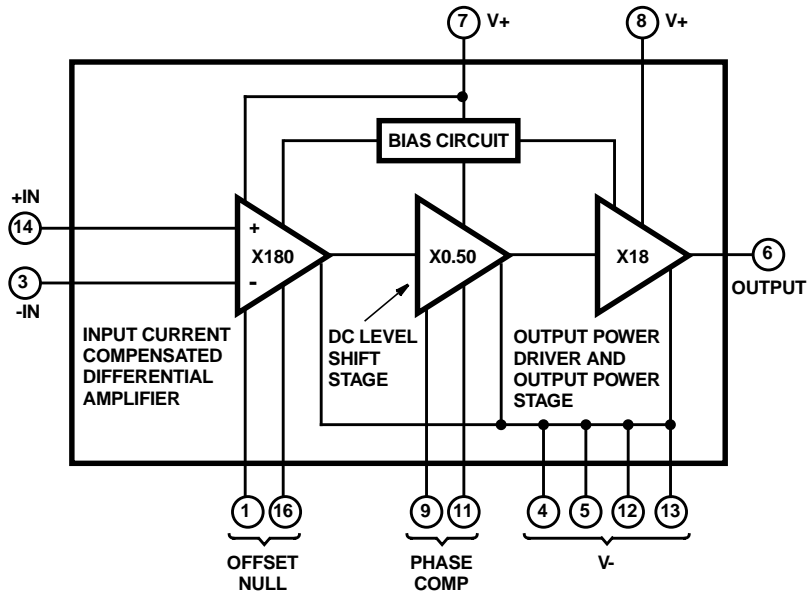
**Applications**

- Video Line Driver
- High Frequency Unity Gain Buffer
- Pulse Amplifier
- High Speed Comparator
- High Frequency Oscillator and Video Amplifiers
- Driver for A/Ds in Video Applications . . . . . 10MHz BW

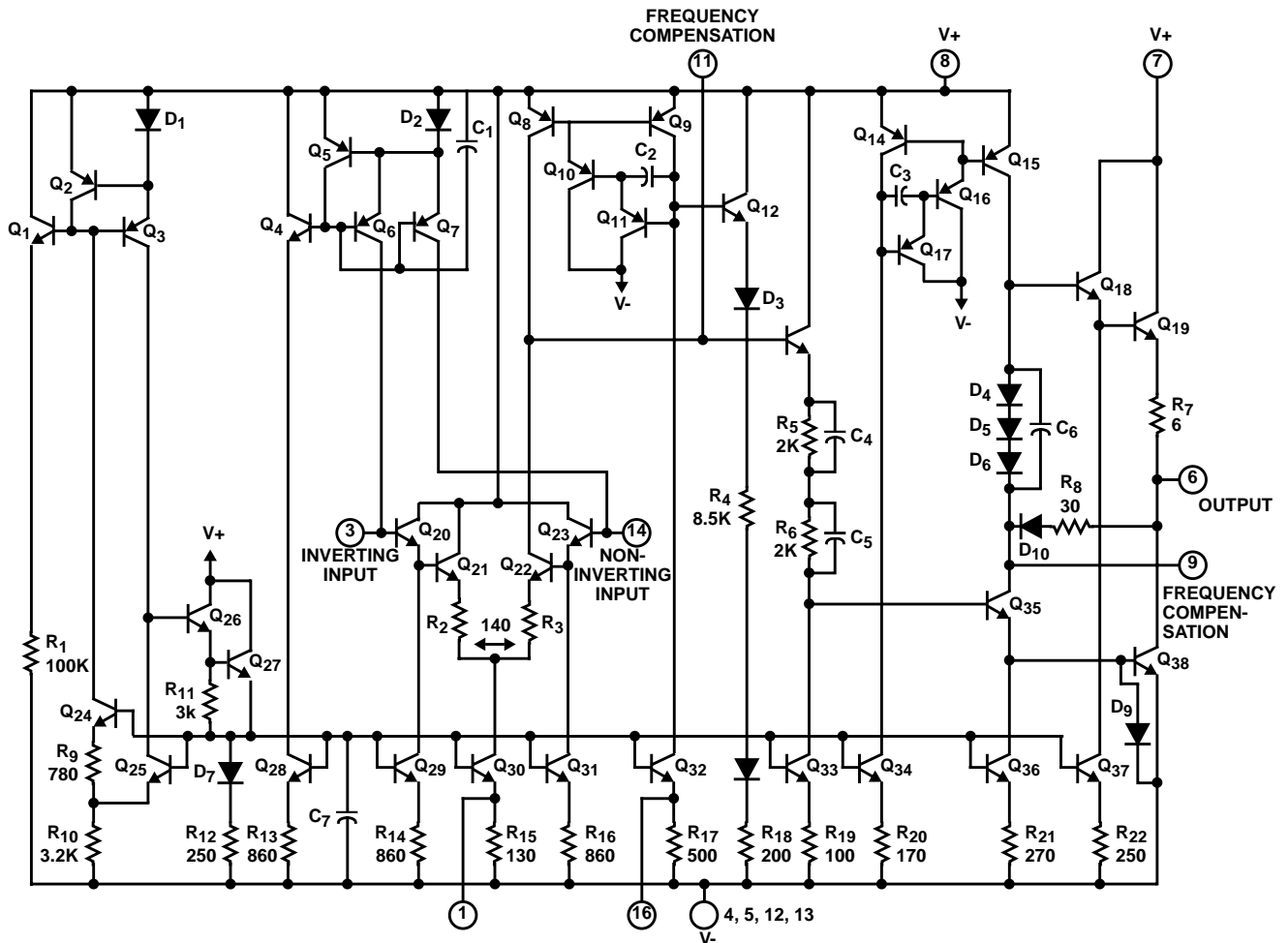
**Part Number Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3450E	-40 to 85	16 Ld PDIP	E16.3

Block Diagram



Schematic Diagram



**Absolute Maximum Ratings**

Supply Voltage (Between V+ and V- Terminals) . . . . . 14.5V  
 Differential Input Voltage . . . . . .5V  
 Output Current . . . . . 100mA

**Operating Conditions**

Temperature Range . . . . . -40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  
 PDIP Package . . . . . 60  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

**Electrical Specifications**  $C_C = 5\text{pF}$ ,  $V_{\text{SUPPLY}} = \pm 6\text{V}$ , Unless Otherwise Specified

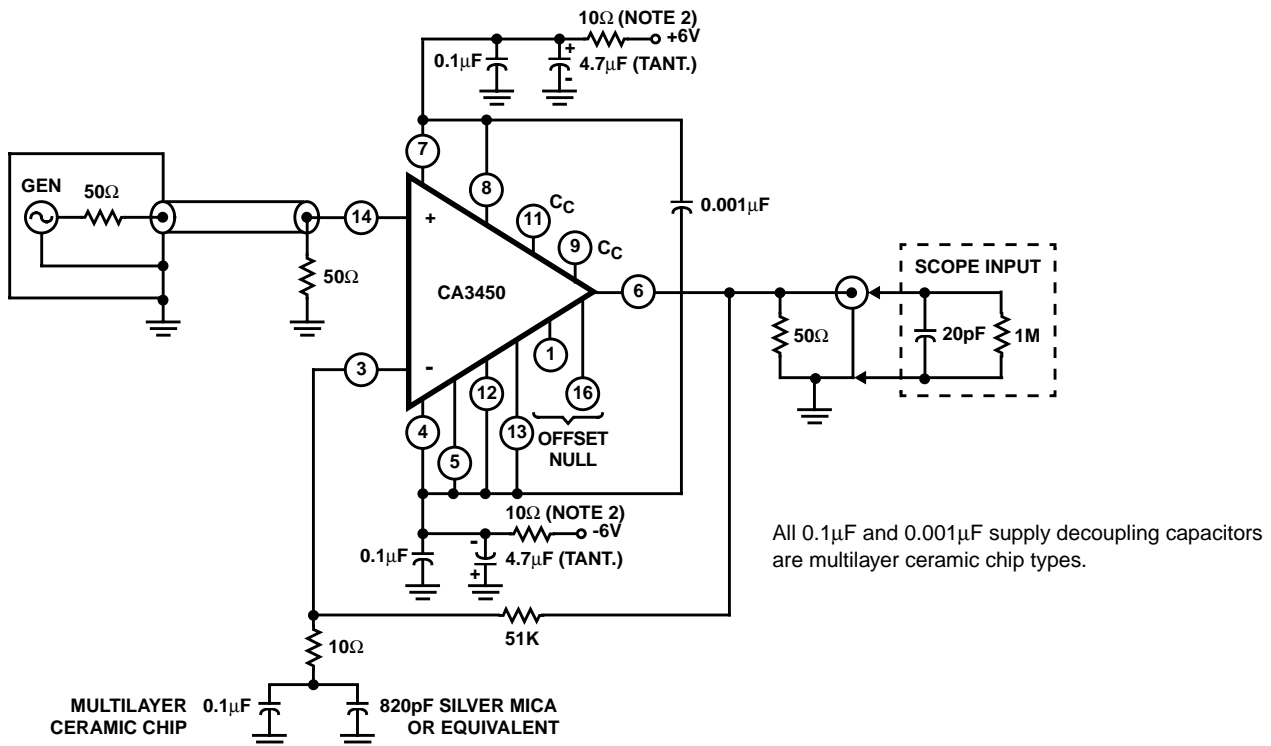
PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS	
<b>DC</b>								
Input Offset Voltage	$ V_{IO} $		25	-	8	20	mV	
			Full	-	10	35	mV	
Input Bias current	$ I_{IB} $		25	-	100	400	nA	
Input Offset Current	$ I_{IO} $		25	-	50	200	nA	
Open Loop DC Gain	$A_{OL}$	$V_{OUT} = \pm 2.5\text{V}$ , $R_L = 50\Omega$	25	60	70	-	dB	
			Full	55	-	-	dB	
Power Supply Rejection Ratio	PSRR	$\Delta V = \pm 1\text{V}$	25	55	65	-	dB	
Common Mode Rejection Ratio	CMRR	$V_{ICR} = \pm 3.5\text{V}$	25	50	60	-	dB	
Common Mode Input Range	$V_{ICR}$		25	$\pm 3.5$	$\pm 3.7$	-	V	
			Full	$\pm 3.0$	-	-	V	
Supply Current	$I_+$		25	-	30	40	mA	
			Full	-	-	50	mA	
<b>DYNAMIC</b>								
-3dB Bandwidth $A_V = 1$ (See Figure 2) $C_C = 5\text{pF}$		No Load	25	-	200	-	MHz	
		$R_L = 1\text{M}\Omega    20\text{pF}$	25	-	190	-	MHz	
		$R_L = 50\Omega    20\text{pF}$	25	-	185	-	MHz	
Bandwidth (Unity Gain Crossing) $A_V = \text{Open Loop}$ $C_C = 0$ (See Figure 1)		No Load	25	210	230	-	MHz	
		$R_L = 20\text{pF}    1\text{M}\Omega$	25	180	200	-	MHz	
		$R_L = 50\Omega    20\text{pF}$	25	180	220	-	MHz	
Bandwidth (Unity Gain Crossing) $A_V = 10$ , $C_C = 0\text{pF}$ $R_{\text{FEEDBACK}} = 450\Omega$ $R_{\text{PIN } 3-G} = 50\Omega$ (See Figure 2)		No Load	25	200	210	-	MHz	
		$50\Omega$	25	175	190	-	MHz	
		$1\text{M}    20\text{pF}$	25	180	195	-	MHz	
		$50\Omega    1\text{M}    20\text{pF}$	25	170	188	-	MHz	
Transient Response, Overshoot (See Figure 3)	OS	$A_V = 1$ , $C_C = 5\text{pF}$	$R_L = 50\Omega    20\text{pF}$	25	-	30	-	%
			No Load	25	-	20	-	%
		$A_V \geq 10$ , $C_C = 0\text{pF}$ , $R_L = 50\Omega    20\text{pF}$	25	-	10	-	%	
Settling Time (See Figure 5) (2V Step, $R_L = 50\Omega    20\text{pF}$ )	$t_S$	$A_V = -1$ , $C_C = 5\text{pF}$ , 0.1%, 10 Bits	25	-	35	-	ns	
		$A_V = 1$ , $C_C = 5\text{pF}$ , 0.1%, 10 Bits	25	-	50	-	ns	
		$A_V = 10$ , $C_C = 0\text{pF}$ , 0.1%, 10 Bits	25	-	35	-	ns	
		$A_V = 10$ , $C_C = 0\text{pF}$ , 1.0%, 7 Bits	25	-	25	-	ns	

# CA3450

## Electrical Specifications $C_C = 5\text{pF}$ , $V_{\text{SUPPLY}} = \pm 6\text{V}$ , Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS	
Slew Rate (See Figures 2, 4)	SR	$A_V = 1$ , $C_C = 5\text{pF}$	No Load	25	-	220	-	V/ $\mu\text{s}$
			$R_L = 50\Omega    20\text{pF}$	25	-	160	-	V/ $\mu\text{s}$
		$A_V \geq 10$ , $C_C = 0\text{pF}$	No Load	25	370	440	-	V/ $\mu\text{s}$
			$R_L = 50\Omega    20\text{pF}$	25	300	330	-	V/ $\mu\text{s}$
Full Power Bandwidth (FPBW = $\text{SR}/\pi V_{\text{P-P}}$ )	FPBW	$A_V = 5$ , $C_C = 5\text{pF}$ $V_{\text{OUT}} = \pm 3.5\text{V}$	No Load	25	-	10	-	MHz
			$R_L = 50\Omega    20\text{pF}$	25	-	7.2	-	MHz
		$A_V \geq 10$ , $C_C = 0\text{pF}$ $V_{\text{OUT}} = \pm 2.0\text{V}$	No Load	25	29	35	-	MHz
			$R_L = 50\Omega    20\text{pF}$	25	24	26	-	MHz
Input Noise Voltage	$e_N$	$f = 1\text{kHz}$	25	-	12	-	nV/ $\sqrt{\text{Hz}}$	
Differential Gain	DG	See Figure 8	25	-	0.2	-	%	
Differential Phase	DP	See Figure 8	25	-	0.2	-	Degrees	
Output Current	$I_{\text{OUT}}$	Into +4V or -4V	25	60	75	-	mA	
Output Voltage Swing	$V_{\text{OM}+}$	$R_L = 75\Omega$	25	3.9	4.1	-	V	
	$V_{\text{OM}-}$		25	-3.9	-4.1	-	V	
Input Capacitance	$C_I$	$f = 1\text{MHz}$	25	-	2.2	-	pF	
Input Resistance	$R_I$		25	-	1	-	M $\Omega$	
Output Resistance	$R_{\text{OUT}}$	See Figure 14, $A_V = 1$ , 30MHz	25	-	4	-	$\Omega$	

## Test Circuits and Waveforms



NOTE:

- A 10 $\Omega$ ,  $\frac{1}{4}\text{W}$  supply decoupling resistor is shown in all application circuits of this device. The resistor serves two purposes. First it provides a means of decoupling the IC directly at its terminal without introducing additional supply resonance due to parallel connected capacitors. Second, it also provides protection for the device in event of a sustained short circuit applied directly to the output terminals.

FIGURE 1. OPEN LOOP GAIN vs FREQUENCY TEST CIRCUIT

Test Circuits and Waveforms (Continued)

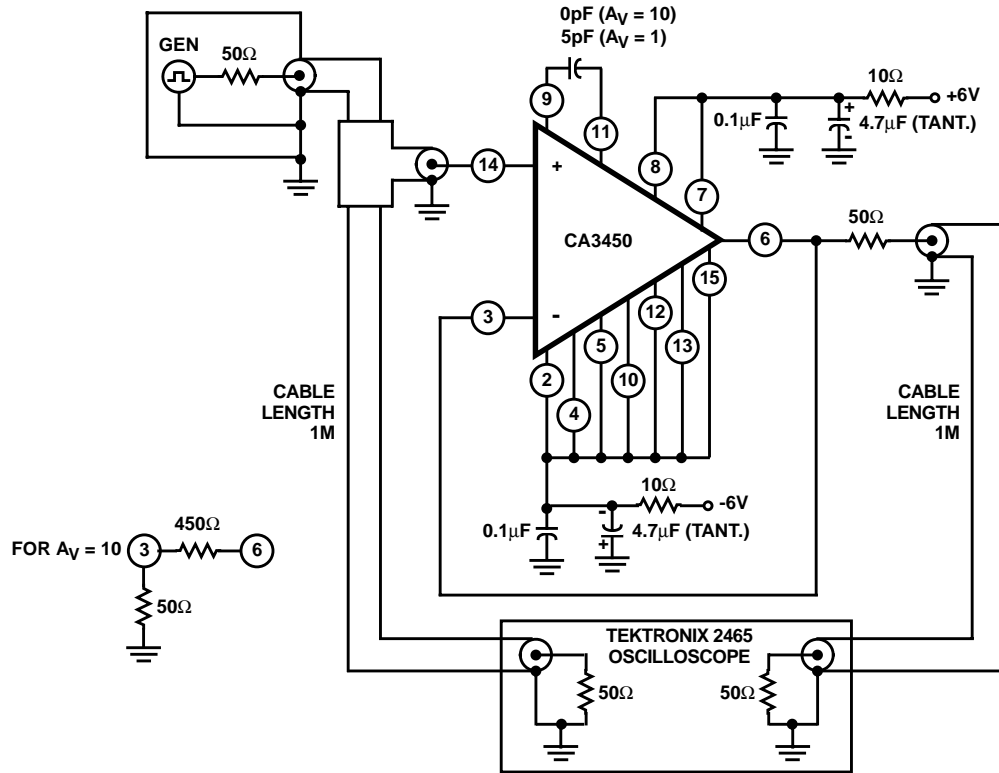


FIGURE 2. UNITY GAIN AND X10 NON-INVERTING AMPLIFIER/AND SLEW RATE TEST CIRCUIT

Transient Response Waveforms

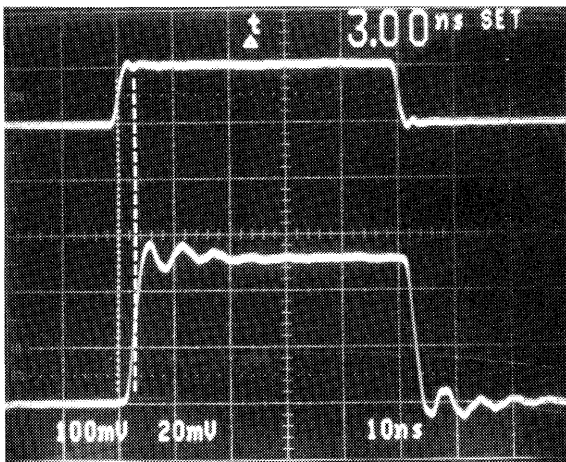


FIGURE 3. TRANSIENT RESPONSE WAVEFORM

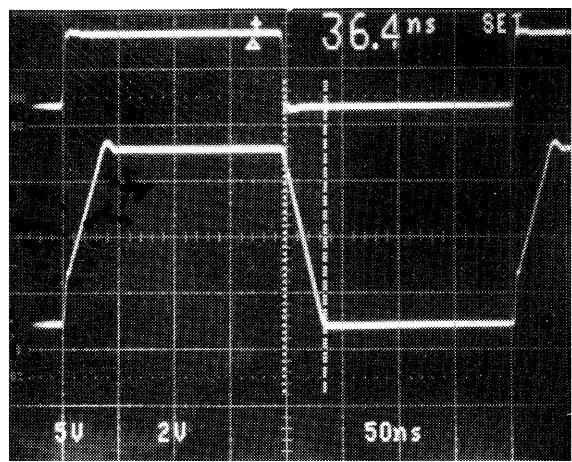


FIGURE 4. SLEW RATE WAVEFORM

Test Circuits and Waveforms (Continued)

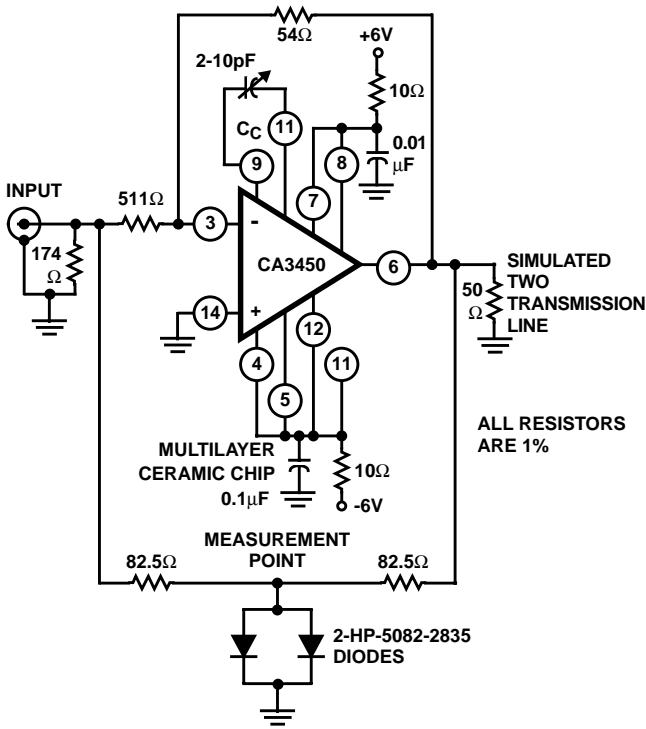


FIGURE 5. CIRCUIT USED TO MEASURE SETTLING TIME

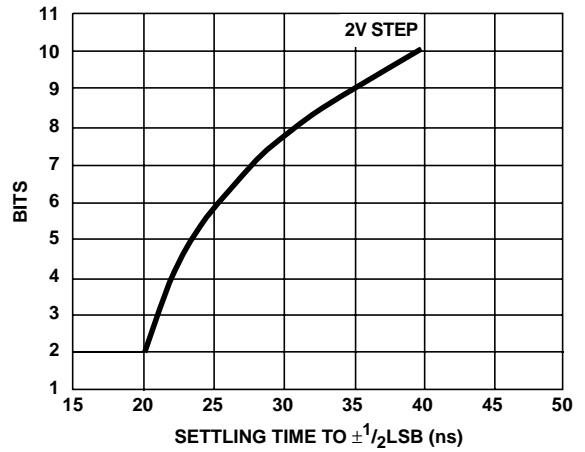


FIGURE 6. ACCURACY IN BITS AS A FUNCTION OF SETTLING TIME

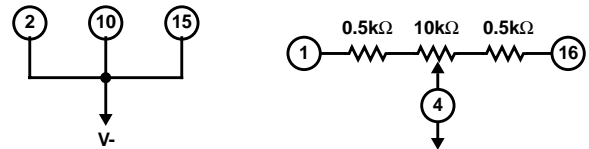


FIGURE 7. NULLING CIRCUIT FOR THE CA3450

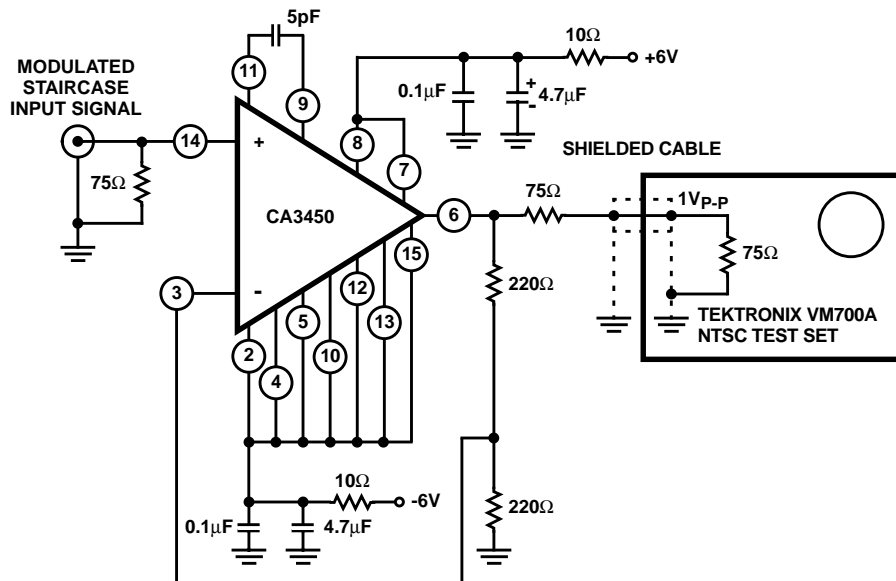


FIGURE 8. CONFIGURATION USED TO MEASURE DIFFERENTIAL GAIN AND PHASE

Test Circuits and Waveforms (Continued)

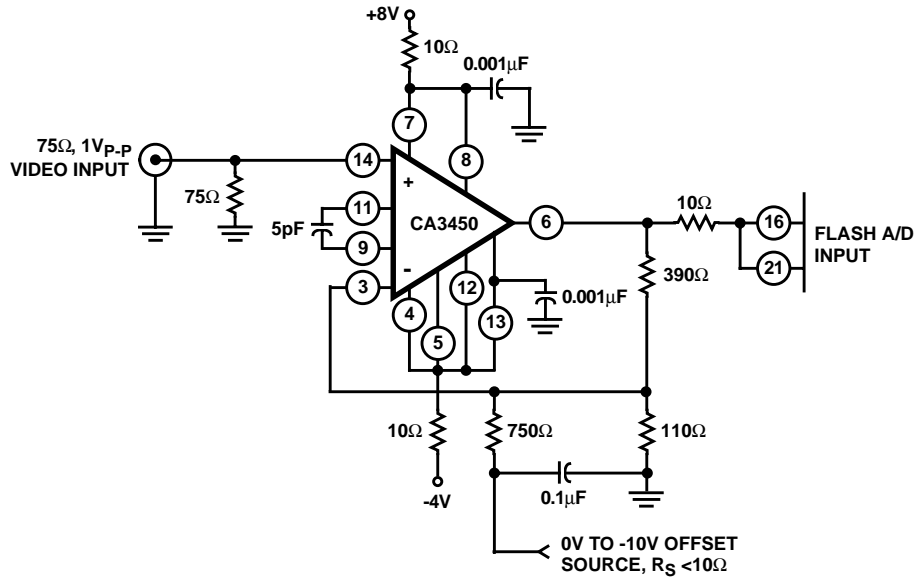


FIGURE 9. TYPICAL HIGH BANDWIDTH X5 AMPLIFIER FOR DRIVING THE CA3318 FLASH A/D

Typical Performance Curves

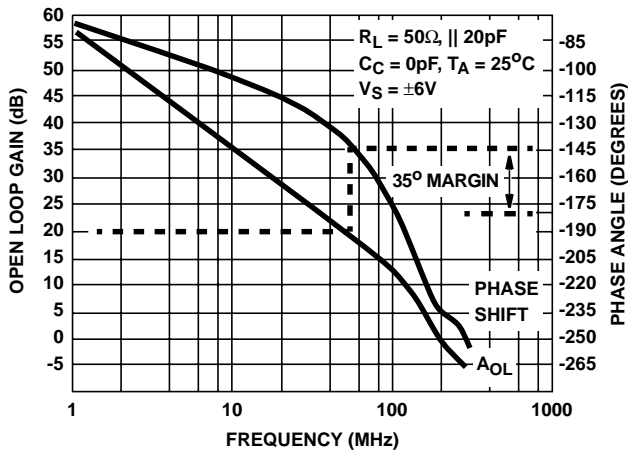


FIGURE 10. BODE PLOT FOR THE CA3450

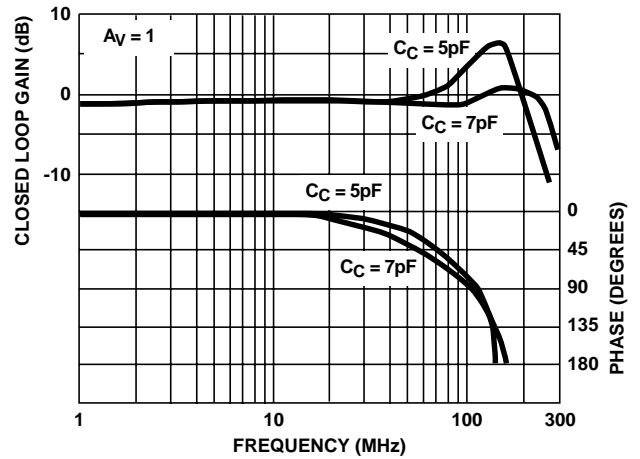


FIGURE 11. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

Typical Performance Curves (Continued)

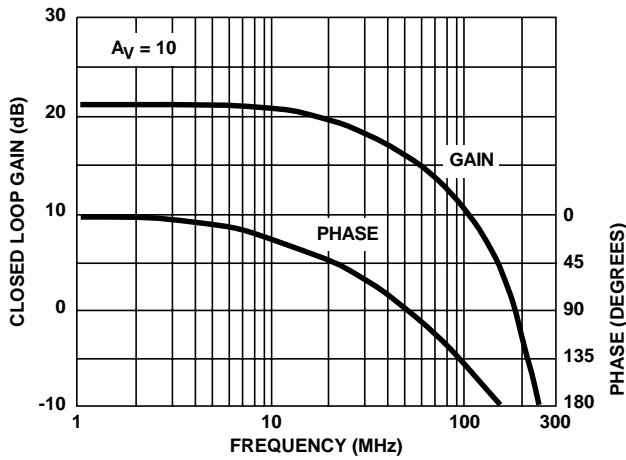


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

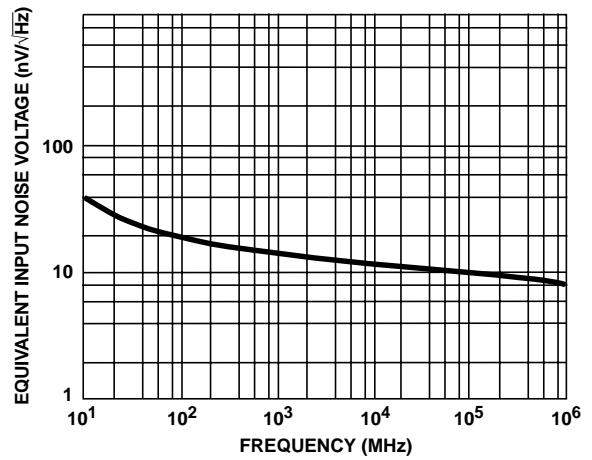


FIGURE 13. EQUIVALENT INPUT NOISE vs FREQUENCY

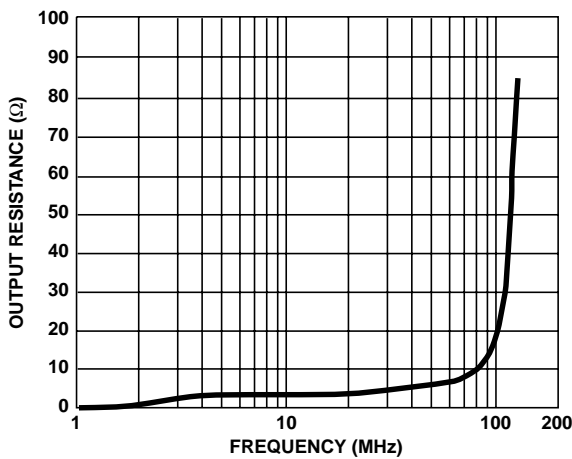


FIGURE 14. OUTPUT RESISTANCE vs FREQUENCY

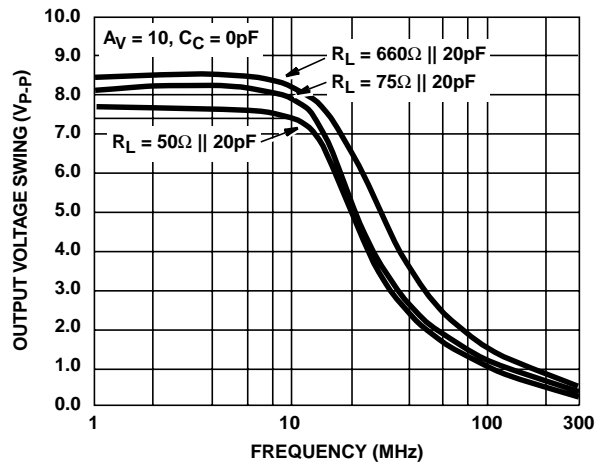
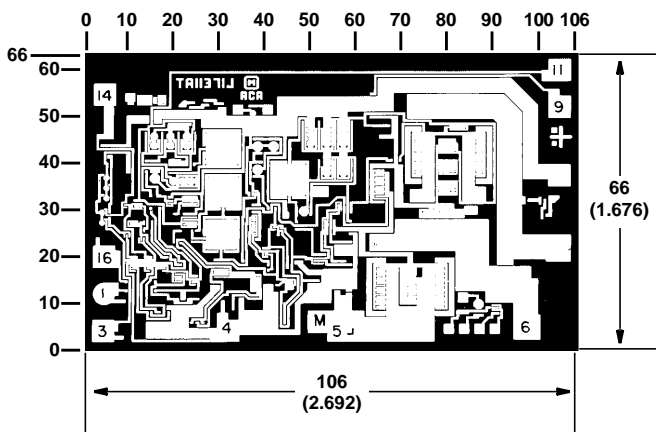


FIGURE 15. OUTPUT VOLTAGE vs FREQUENCY

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3mils to +6mils applicable to the nominal dimensions shown.